AXPM450xxyz

150/300/500mA, Low VIN, Low VOUT Ultra-low Dropout NMOS Regulator

Preliminary Datasheet — Feb 2022

Description

AXPM450xxyz is a high accuracy, low quiescent current and ultra-low dropout regulator (LDO) that can source 500mA. Its NMOS pass transistor is biased by a dedicated VBIAS pin allowing for ultra-low dropout performance at very low input voltages.

This enables increased efficiency and together with its low quiescent current, AXPM450xxyz is ideal for low power battery-operated, power-sensitive applications. Short circuit current foldback and thermal protection are included. It can be stabilized with a small capacitor at the output, saving on space overheads.

An enable logic control function puts AXPM450xxyz in shutdown mode, enabling a total current consumption of less than 0.1μA. Device options allows for active pull down at the output for discharge when disable.

Features

- Input voltage range: 0.8V to 5.5V
- Low quiescent current 25μA (typ) at no load
- Ultra-low dropout 75mV (typ) at 500 mA
- Available in 8 fixed-output voltages: 0.8V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V
- ±1% VOUT accuracy over Temperature
- High PSRR: 60dB at 1kHz
- Short circuit current limit with foldback
- Thermal shutdown

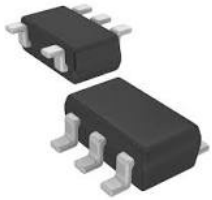
Applications

- Camera supply
- Mobile phones
- Tablets
- Battery-powered systems

Table 1 Device Summary

Order code	
AXPM450xxyz	xx: 08=0.8V, 10=1.0V, 12=1.2V, 15=1.5V, 18=1.8V, 25=2.5V, 28=2.8V, 30=3.0V. y: K=DFN4 epad N=SOT23-5L z: 1=150mA 2=300mA 3=500mA

DFN4 epad
(1.0 x 1.0 x 0.37)



SOT23-5L
(2.9 x 1.6 x 1.1)

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Figure 1 Block Diagram

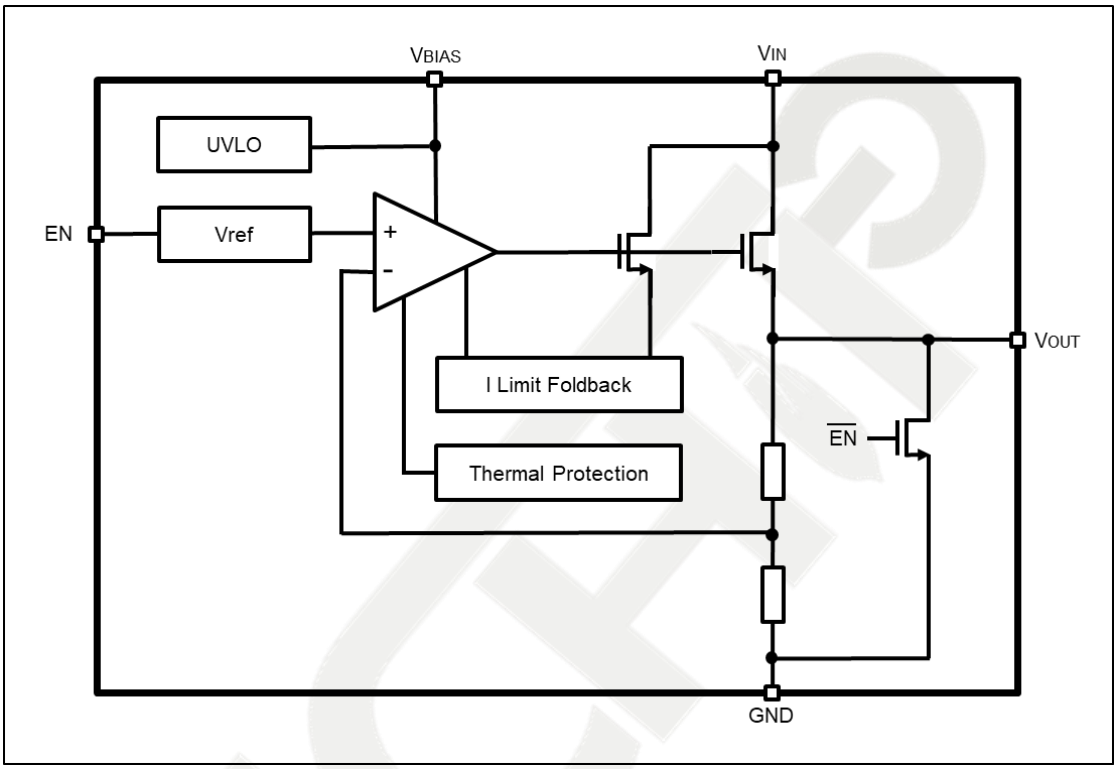
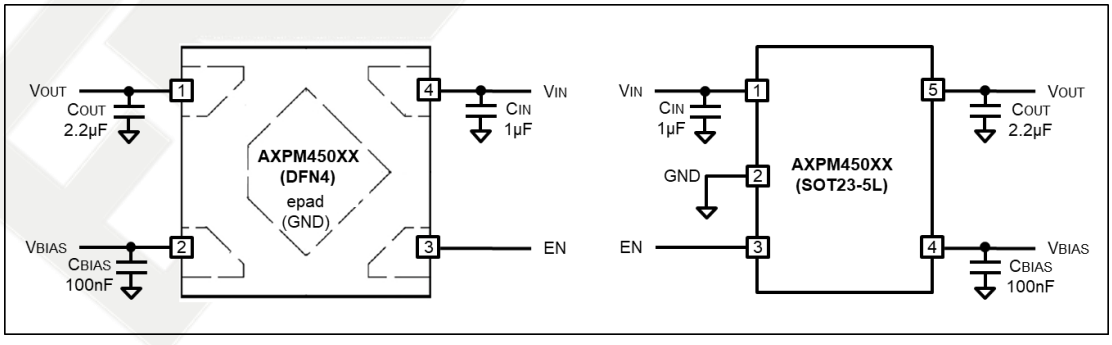


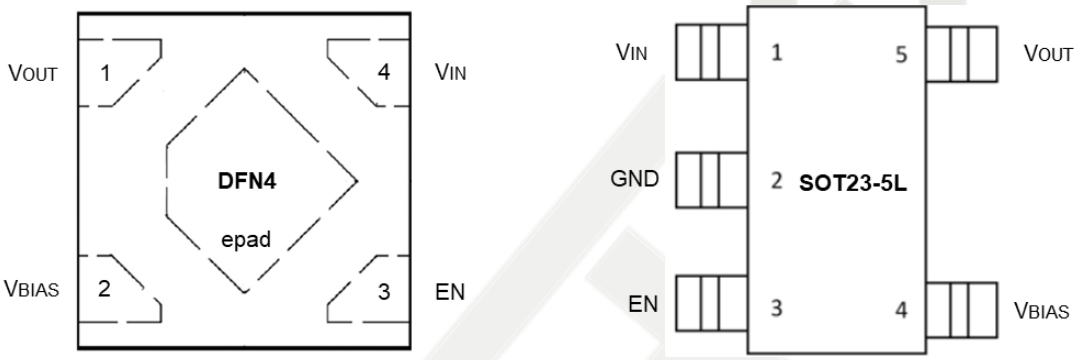
Figure 2 Application Circuit



2 Pin Description

2.1 Pin Names

Figure 3 Pin Connection



2.2 Pin Functions

Table 2 Pin Functions

Pin number (DFN)	Pin number (SOT23-5)	Pin name	Description
1	5	VOUT	Output voltage
2	4	VBIAS	Bias supply input
3	3	EN	Enable pin logic input: low=shutdown, high=active.
4	1	VIN	Input supply voltage
epad	2	GND	Ground

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	-0.3 to +7	V
V_{BIAS}	Input voltage (for driver)	-0.3 to +7	V
V_{OUT}	Output voltage	-0.3 to V_{IN}+0.3	V
V_{EN}	Enable input voltage	-0.3 to +7	V
I_{OUT}	Output current	Internally limited	mA
PD	Power dissipation	Internally limited	mW
Tj	Junction temperature	+150	°C
Tstg	Storage temperature range	-55 to +150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. The functional operation at or over these absolute maximum ratings is not assured.

3.2 Thermal Data

Table 4 Thermal Data

Symbol	Parameter		Value	Unit
Rth j-amb	Thermal resistance junction-to-case	DFN4	60	°C/W
		SOT23-5L	70	°C/W
Rth j-case	Thermal resistance junction-to-ambient	DFN4	250	°C/W
		SOT23-5L	260	°C/W

3.3 ESD and Latch Up

Table 5 ESD and Latch Up

Symbol	Parameter		Value	Unit
All pins	Electronics Static Discharge protection voltage	HBM	±2,000	V
		CDM	±500	V
All pins	Latch Up JESD78, Class A		≥ 100	mA

3.4 Electrical Characteristics

V_{BIAS} = 2.7V or V_{OUT} + 1.6V (whichever is greater); V_{IN} = V_{OUT} + 0.3V; I_{OUT} = 1mA; C_{IN} = 1μF, C_{OUT} = 2.2μF; V_{EN} = 1V; typical values are at Tamb = 25°C; min/max values are at -40°C ≤ Tamb ≤ 85°C, unless otherwise specified.

Table 6 Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating input voltage		V_{OUT} + V_{DROP}		5.5	V
V_{BIAS}	Operating bias voltage	V_{OUT} ≤ 1V	2.4		5.5	V
		V_{OUT} > 1V	V_{OUT} + 1.4		5.5	V
T_{OP}	Operating temperature		-40		+85	°C
V_{UVLO}	BIAS under-voltage lockout	V_{BIAS} rising		1.6		V
		Hysteresis		0.2		
V_{OUT}	Output voltage accuracy		-0.5		+0.5	%
		V_{OUT} (nom) + 0.3V ≤ V_{IN} ≤ V_{OUT} (nom) + 1V; 2.7V or V_{OUT} (nom) + 1.6V (whichever is greater) ≤ V_{BIAS} ≤ 5.5V; I_{OUT} = 1mA to 500mA; -40°C ≤ Tamb ≤ 85°C	-1.5		+1.5	%
ΔV_{OUT}-IN	V_{IN} line regulation (1)	V_{OUT} (nom) + 0.3V ≤ V_{IN} ≤ 5V; I_{OUT} = 1mA		0.02	0.1	%/V
ΔV_{OUT}-BIAS	V_{BIAS} line regulation (1)	2.7V or V_{OUT} (nom) + 1.6V (whichever is greater) ≤ V_{BIAS} ≤ 5.5V; I_{OUT} = 1mA		0.01	0.1	%/V
ΔV_{OUT}	Static load regulation	I_{OUT} = 1mA to 500mA		1.5		mV
V_{DROP}	Dropout voltage	I_{OUT} = 150mA; V_{OUT} = 97% of V_{OUT} (nom)		25	75	mV
		I_{OUT} = 500mA; V_{OUT} = 97% of V_{OUT} (nom)		80	250	
V_{DROP}-BIAS	Dropout voltage	V_{BIAS} = V_{IN}; I_{OUT} = 500mA		0.9	1.5	V
Vn	Output noise voltage	V_{OUT} (nom) = 1.05V; V_{IN} = 1.5V 10Hz to 100kHz; I_{OUT} = 1mA		38		μV rms
SVR_{IN}	V_{IN} supply voltage rejection	V_{IN} = V_{OUT} (nom) + 0.5V ± V_{RIPPLE}; V_{RIPPLE} = 0.2V, 1kHz; I_{OUT} = 150mA;		75		dB

		V_{BIAS} = 2.7V or V_{OUT} + 1.6V (whichever is greater)				
SVR_{BIAS}	V_{BIAS} supply voltage rejection	V_{BIAS} = 2.9V or V_{OUT} + 1.8V (whichever is greater) ± V_{RIPPLE}; V_{RIPPLE} = 0.2V, 1kHz; I_{OUT} = 150mA; V_{IN} = V_{OUT} (nom) + 0.5V		76		dB
I_{BIAS}	V_{BIAS} operating current	I_{OUT} = 0; V_{BIAS} = 2.7V		27	40	μA
IStby-BIAS	V_{BIAS} standby current	V_{BIAS} input current in OFF MODE: V_{EN} = GND		0.03	1	μA
IStby-IN	V_{IN} standby current	V_{IN} input current in OFF MODE: V_{EN} = GND		0.03	1	μA
I_{LIM}	Output current limit	V_{OUT} = 0.9 x V_{OUT} (nom)	550	700	1,000	mA
I_{SC}	Short circuit current	V_{OUT} = 0 (foldback protection)		365	500	mA
R_{ON}	Output discharge mosfet			110		Ω
V_{EN}	Enable logic low				0.4	V
	Enable logic high		0.9			
I_{EN}	Enable input current	V_{EN} = 5.5V			400	nA
T_{ON} (2)	Turn on time	V_{OUT} (nom) = 1V		110		μs
T_{SD}	Thermal shutdown			160		°C
	Hysteresis			20		°C
C_{OUT}	Output capacitor		1	2.2	22	μF

(1) Not applicable for V_{OUT} (nom) ≥ 5V.
(2) Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 98% of its nominal value.

4 Functional Description

4.1 V_{BIAS} Voltage Requirement

V_{BIAS} is used for the driving of the NMOS pass channel. The pin must have a minimum voltage of 2.4V and 1.6V (typically) higher than the output for proper operation. In the event V_{IN} supply is meeting the bias requirement, V_{BIAS} can be connected directly to V_{IN}.

4.2 Output Discharge Function

A discharge mosfet is available at V_{OUT} for quick discharge of the output capacitor when device is disabled (EN = low). Optional devices are also available without this discharge mosfet function.

4.3 Short Circuit and Current Limitation

Short circuit current limit foldback protection is integrated. The load current is limited to I_{LIM} when V_{OUT} is equal to 90% of its nominal value. On further decreasing V_{OUT} due to low impedance short circuit, foldback circuit starts operating, limiting the current to I_{SC} when V_{OUT} = 0.

4.4 Thermal Protection

AXPM450xxyz is protected with thermal shutdown when the junction temperature reaches 160°C typical. It recovers upon cooling and reaching thermal hysteresis value.

4.5 Input and Output Capacitors

External capacitors are required to ensure the regulator control loop stability. For the input and outputs capacitors, a minimum of 1µF for C_{IN}, a minimum of 100nF for C_{BIAS} and a minimum of 1µF (with ESR 3 to 300mΩ) for C_{OUT} are required.

Good quality ceramic capacitors such as the X5R and the X7R are suggested. Further care in placing capacitors close to the pins with low impedance routing and with good return Analog ground minimization of noise pickup. Along with good capacitors having low variations across operation conditions, excellent performance can be achieved with AXPM450xxyz.

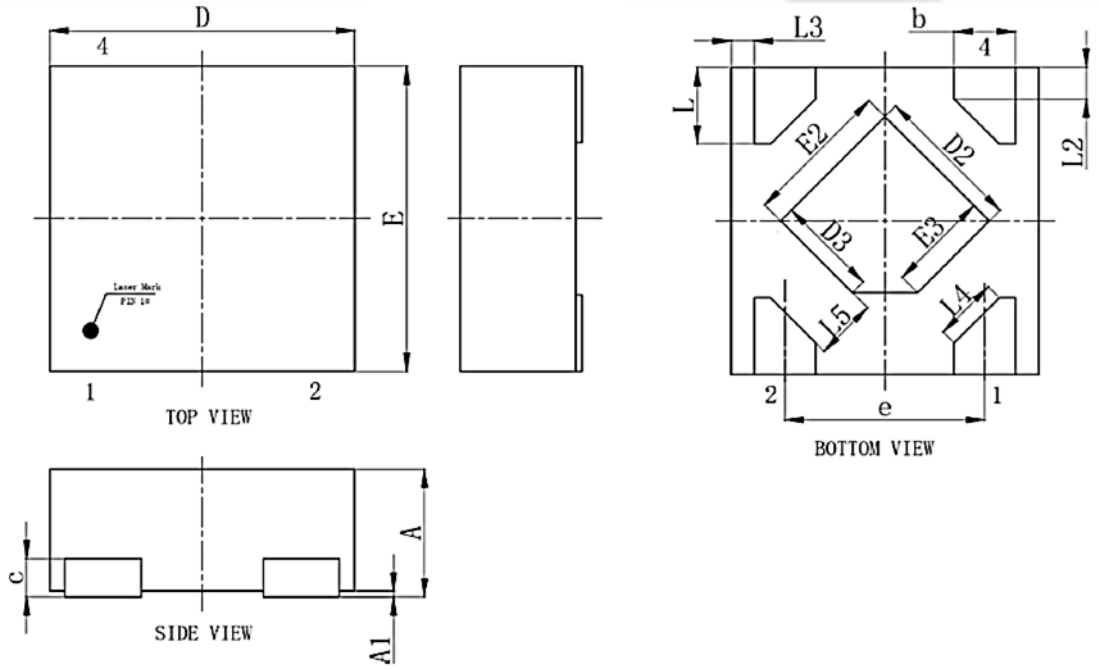
4.6 Under-voltage Lockout (UVLO)

An under-voltage lockout function for V_{BIAS} is included. On powering up, lockout is maintained till V_{BIAS} reaches 1.6V. A hysteresis of 0.2V is designed in to ensure clean entry and exit from the lockout.

5 Package Information

5.1 DFN4

Figure 4 DFN4 EPAD 1.0 x 1.0 x 0.37 Mechanical Data and Package Dimensions

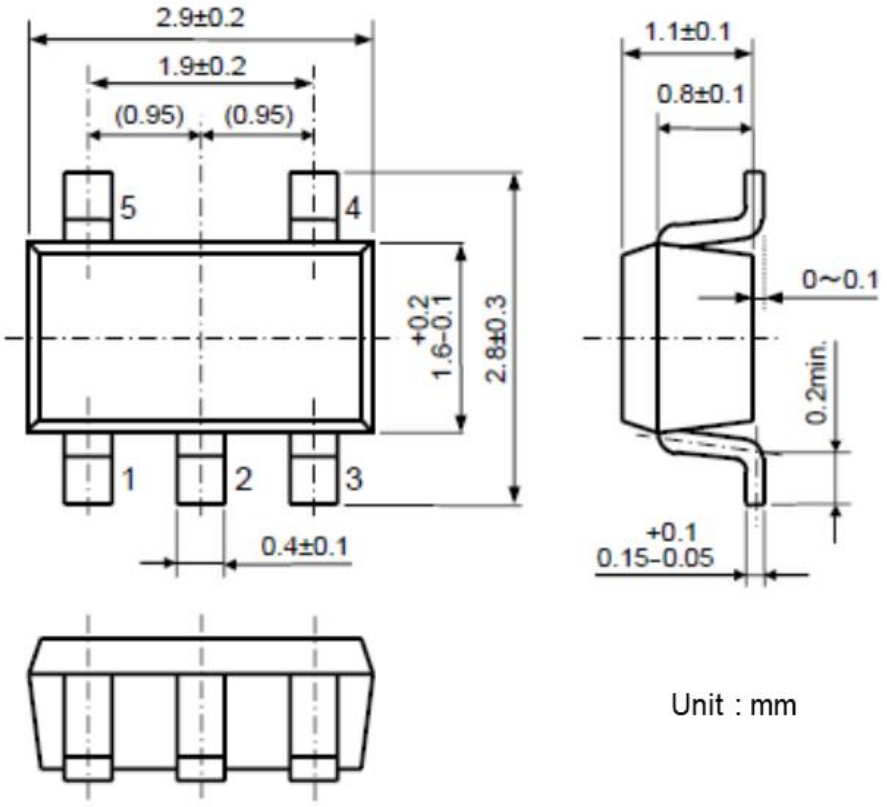


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.127REF		
D	0.95	1.00	1.05
D2	0.38	0.48	0.58
D3	0.23	0.33	0.43
e	0.65BSC		

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
E	0.95	1.00	1.05
E2	0.38	0.48	0.58
E3	0.23	0.33	0.43
L	0.20	0.25	0.30
L2	0.103REF		
L3	0.075REF		
L4	0.208REF		
L5	0.200REF		

5.2 SOT23-5L

Figure 5 SOT23-5L 2.9 x 1.6 x 1.1 Mechanical Data and Package Dimensions



6 Revision History

Table 7 Document Revision History

Date	Version	Description
Jun 2020	Draft	Preliminary Version